REMARKS

Status of the Claim

Claims 1-12, 18, 19 were previously cancelled.

Claims 13-17, 20, 21, 23, 24 have been rejected.

Claim 22 has been objected to.

By this response, **claims 13, 15-17, 20-24 have been amended**.

Response to Examiner's Office Action.

The Examiner rejected claims 13, 15-17, 20, 21 and 24 under 35USC103(a) as being anticipated by Christeson U.S. No. 6,622,243 in view of Ellis US Pub. 2002/0087886.

The Examiner stated;

"As per claims 13, 14, 17, 20, 21 and 24, Figure 1 of Christeson is directed to a memory back-up system comprising: a volatile memory cell (101); a non-volatile cell (102) that is interfaced with the volatile memory cell; a common control line (104) connected to the volatile memory cell and the non-volatile memory cell, the control line allowing data to be simultaneously written to the volatile memory cell and the non-volatile memory cell (col. 3, lines 21-29).

The Examiner further states that Christeson is silent about the non-volatile memory cell being integrated with the volatile memory cell; and the non-volatile memory cell is an MRAM cell and the volatile memory cell is a DRAM memory cell. The Examiner further claims paragraph [0101] of Ellis discloses a non-volatile memory cell being integrated with a volatile memory, and that the non-volatile memory cell is an MRAM memory cell and the volatile memory cell is a

DRAM memory cell. The Examiner claims that it would be obvious that Christeson could have the MRAM non-volatile memory cell being integrated with the DRAM volatile memory cell as taught by Ellis in order to improve the efficient operation of the microprocessor in the computer system.

Amended claim 13 includes the following features:

> a volatile memory cell;
>
> a non-volatile memory cell, the non-volatile memory cell being integrated with the volatile memory cell, the non-volatile memory cell being interfaced with the volatile memory cell;
>
> a single word line WL connected to the integrated volatile memory cell and the non-volatile memory cell, the single word line WL allowing data to be simultaneously written to the volatile memory cell and the non-volatile memory cell.
>
> (Emphasis Added)

Support for the amendment of claim 13 can be found throughout the specification. For example, old claim 22 included a single word line WL is connected to both the first memory cell and the non-volatile memory cell.

Claim Rejections – 35 U.S.C. § 103(a)

For the purpose of the following discussion, the Examiner is respectfully reminded of the basic considerations which apply to obviousness rejections.

> When applying 35 U.S.C. §103, the following tenets of patent law must be adhered to:
>
> (A) The Claimed invention must be considered as a whole;
>
> (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;
>
> (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the Claimed invention; and
>
> (D) Reasonable expectation of success is the standard with which obviousness is determined. MPEP §2141.01, *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1134 n.5, 229 U.S.P.Q. 182, 187 n.5 (Fed. Cir. 1986).

In addition, it is respectfully noted that to substantiate a *prima facie* case of obviousness the initial burden rests with the Examiner who must fulfill three requirements. More specifically:

> To establish a *prima facie* case of obviousness, three basic criteria must be met.
>
> **First**, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings.
>
> **Second**, there must be a reasonable expectation of success.
>
> **Finally**, the prior art reference (or references when combined) must teach or suggest all the Claim limitations. The ***teaching or suggestion*** to make the Claimed combination **and** the ***reasonable expectation of success*** **must** ***both be found in the prior art,*** **and not** ***based on Applicant's disclosure***. (emphasis and formatting added) MPEP § 2143, *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)

The Examiner has rejected Claims 13, 15-17, 20, 21 and 24 as being allegedly unpatentable over Christeson in view of Ellis. Applicant respectfully disagrees and traverses the rejection. Applicant includes herein by reference each and every statement made above, in addition these Claims are also patentable for the following additional reasons.

Paralleling the MPEP references cited above, the Federal Circuit has enunciated several guidelines in making a §103 obviousness determination. A *prima facie* case of obviousness is established when and only ***when the teachings from the prior art itself*** would appear to have ***suggested*** the Claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051 (C.C.P.A. 1976)). (Emphasis added). "The mere fact that the prior art ***may*** be modified in the manner suggested by the Examiner does ***not*** make the modification obvious unless the prior art suggested the desirability of the modification." (emphasis added) *In re Fritch*, 23 U.S.P.Q.2d 1780, 1783-84 (Fed. Cir. 1992).

The embodiments of Christeson include a processor 100, CMOS memory 101, and a non-volatile memory 102. The components communicate with each other over bus 104. The non-volatile memory preferable is flash memory. (Col. 2, lines 31-48).

Christeson does not provide features of the claimed invention. More specifically, Christeson does not provide non-volatile memory cell being integrated with the volatile memory cell. Additionally, Christeson does not provide a single word line WL connected to the integrated volatile memory cell and the non-volatile memory cell, the common control line allowing data to be simultaneously written to the volatile memory cell and the non-volatile memory cell.

Figure 1 clearly shows the CMOS memory and the non-volatile flash memory as two separate pieces of memory. The two separate pieces of memory require a data bus 104 for transferring data between the two separate pieces of memory. Christenson does not teach, describe or even suggest the desirability of integrating the non-volatile and volatile memory cells. The integration of the two types of memory allows a large amount of data to be transferred between the two types of memory efficiently (see applicant's specification page 14, lines 13-16).

Christenson teaches a preferred embodiment (Col. 3, lines 21-26) that includes an exit and same routine that further include computer-executable instructions, which cause new configuration information to be automatically stored in non-volatile memory 102 at the same time it is written into CMOS memory. Christenson clearly states that it is the computer-executable instructions which cause the configuration information to be written to both memory types at the same time. There is no way that computer-executable instructions can be construed to teach integration of the two types of memory, or a single word line WL to the two types of memory. There is absolutely no requirement that computer-executable instructions causing information to be written to two types of memory have common control lines.

Christenson shows a data bus 104 connecting the CMOS memory 101 and the Non-volatile memory 102. A data bus 104 is used to distribute data between devices.

Data buses are not used for controlling memory or devices connected to the data bus. There is absolutely no discussion by Christenson regarding the controls for reading or writing data to the CMOS memory or the Non-volatile memory. Therefore, there is no way to conclude that word lines are shared between the two types of memory. The memory types suggested by Christenson include CMOS memory and flash memory. There is no suggestions whatsoever of using common controls for the CMOS memory and the flash memory.

Paragraph [0121] of Ellis provides the only reference to the integration of volatile and non-volatile memory, and includes the statement "... integration of volatile memory (RAM like DRAM or equivalent) , or non-volatile memory (like flash, or magnetic, such as MRAM, or ovonic memory), on the "system on a chip" microchip obviates an increasingly unwieldy number of microchip connection prongs, ... " Ellis makes absolutely no reference to control lines, word lines or the transfer of data between volatile and non-volatile memory.

Therefore, there is no way to conclude that Chrisenson in combination with Ellis teaches the claimed invention. All of the claimed elements are not taught, and ***the teachings from the prior art itself*** do not ***suggest*** the Claimed subject matter. Claims 13, 15-17, 20, 21 and 24 are patentable over the cited prior art.

Regarding claim 15, the Examiner stated:

> "Christenson is silent to disclose further comprising a second control line which in combination with the common control line provides selection of the volatile memory cell. However, this feature is seen to be an inherent teaching of the device since a means for providing a process of the system is disclosed and it is apparent that some type of control lines such as a control word line or control column must be present to select the volatile memory cell for the system to function as intended. For example, Christenson in column 2, lines 45-47 discloses that the volatile memory cell is a random access memory device, whose memory cell location needs the control word line and control column line to select the memory cell location as being understood by those skilled in the art."

Applicants respectfully disagree with the Examiner's rejection of claim 15. Claim 15 is dependent on claim 13 and should therefore be allowed. However, as explained above, there is no suggestion by Christenson to provide a common control line. Therefore, there is no way that Christenson suggests a second control line which in combination with the a single word line WL connected to the integrated volatile memory cell and the non-volatile memory cell, because Christenson provides no suggestion of a a single word line WL connected to the integrated volatile memory cell and the non-volatile memory cell.

Regarding claim 16, the Examiner stated:

> "Christenson is silent to disclose further comprising a third control line which in combination with the common control line provides selection of the non-volatile memory cell. However, this feature is seen to be an inherent teaching of the device since a means for providing a process of the system is disclosed and it is apparent that some type of control lines such as a control word line or control column must be present to select the volatile memory cell for the system to function as intended. For example, Christenson in column 2, lines 48 discloses that the non-volatile memory cell is a flash memory device, whose memory cell location needs the control word line and control column line to select the memory cell location as being understood by those skilled in the art."

Applicants respectfully disagree with the Examiner's rejection of claim 16. Claim 16 is dependent on claim 13 and should therefore be allowed. However, as explained above, there is no suggestion by Christenson to provide a common control line. Therefore, there is no way that Christenson suggests a third control line which in combination with the a single word line WL connected to the integrated volatile memory cell and the non-volatile memory cell provides selection of the volatile memory cell, because Christenson provides no suggestion of a single word line WL connected to the integrated volatile memory cell and the non-volatile memory cell.

Claims 17, 20, 21 were rejected for the same reason as set forth in claims 13, 15 and 16.

Claims 17 is dependent on claim 13. Therefore, claim 17 should be allowed. Independent claims 20, 21 include the similar features as claim 13. Therefore, claims 20 and 21 should be allowed.

The Examiner has indicated the claim 22, 23 should be allowable.

No new matter has been added by these amendments.

CONCLUSION

For the reasons given above, and after careful review of all the cited references, Applicant respectfully submits that none of the cited references, nor any combination of the cited references, will result in, teach or suggest Applicant's Claimed invention. But even if any such combination might arguably result in such Claimed invention, it is submitted that such combination would be non-obvious and patentable.

In view of the above Amendments and Remarks, Applicant has addressed all issues raised in the Office Action dated September 01, 2004, and respectfully solicits a Notice of Allowance for Claims 13-17, 20-24. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

It is believed that all of the pending Claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending Claims (or other Claims) that have not been expressed. Finally nothing in this paper should be construed as an intent to concede any issue with regard to any Claim, except as specifically stated in this paper, and the amendment of any Claim does not necessarily signify concession of unpatentability of the Claim prior to its amendment.

Applicant believes that no fees are currently due; however, should any fee be deemed necessary in connection with this Amendment and Response, the Commissioner is authorized to charge deposit account 08-2025, referencing the Attorney docket number 100201070-6.

Respectfully submitted,
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